

WHAT IS CLAIMED IS:

1. A method of synchronizing a receive clock signal phase of a receiving channel with a transmit clock signal phase of a transmitting channel in a transceiver, the method comprising:
 - storing a previous receive clock signal phase of the receiving channel;
 - identifying a current receive clock signal phase of the receiving channel;
 - determining a phase difference between the previous receive clock signal phase and the current receive clock signal phase;
 - identifying a direction of the phase difference between the previous receive clock signal phase and the current receive clock signal phase; and
 - adjusting a previous transmit clock signal phase of the transmitting channel to a current transmit clock signal phase of the transmitting channel based on the phase difference and the direction.
2. The method of claim 1, wherein the storing step, the identifying a current receive clock signal phase step, the determining step, and the identifying a direction step occur at the receiving channel.
3. The method of claim 1, further including the step of providing the phase difference and the direction to the transmitting channel,
wherein the adjusting step occurs at the transmitting channel.
4. The method of claim 3, wherein the adjusting step includes:
 - on a receive clock signal pulse, receiving and writing the phase difference and direction to a retiming module; and
 - on a transmit clock signal pulse, reading out from the retiming module new transmit clock phase data based on the phase difference and direction.

5. The method of claim 3, wherein during the providing step the phase difference and direction is provided to the transmitting channel in an N-bit sequence with the phase difference represented in binary format within a first portion of the N-bit sequence and the direction is provided in a second portion of the N-bit sequence.
6. The method of claim 5, wherein the second portion is a 1 if the phase direction is backward and a 0 if the phase direction is forward.
7. The method of claim 5, wherein the second portion is a 0 if the phase direction is backward and a 1 if the phase direction is forward.
8. The method of claim 1, wherein the storing step and the identifying a current receive clock signal phase step occur at the receiving channel.
9. The method of claim 1, further including the step of providing the previous receive clock signal phase and the current receive clock signal phase to the transmitting channel,
wherein the storing step, the determining step, the identifying a direction step, and the adjusting step occur at the transmitting channel.
10. The method of claim 9, wherein the providing step includes, on receive clock signal pulses, receiving and writing the previous receive clock signal phase and the current receive clock signal phase to a retiming module of the transmitting channel.
11. The method of claim 9, wherein the adjusting step includes, on a transmit clock signal pulse, reading out from a retiming module of the transmitting channel new transmit clock phase data based on the current receive clock signal phase and the previous receive clock signal phase.

12. The method of claim 1, wherein each receive clock signal phase is equivalent to one of plurality of phases that have a constant offset between them.
13. The method of claim 1, wherein the determining step further includes the step of determining if the phase difference exceeds a predetermined phase difference threshold.
14. The method of claim 1, wherein the receiving channel and the transmitting channel are each part of a common lane.
15. The method of claim 1, wherein the receiving channel and the transmitting channel are each part of a different lane of a common core.
16. The method of claim 1, wherein the receiving channel and the transmitting channel are each part of a different core disposed on a common substrate.
17. The method of claim 1, wherein the receiving channel and the transmitting channel are each part of a different core disposed on different substrates.
18. The method of claim 1, wherein the receiving channel and the transmitting channel are each part of a different core disposed on different substrates on different boards.

19. A system for synchronizing a receive clock signal phase with a transmit clock signal phase, the system comprising:

a receiving channel; and

a transmitting channel,

wherein the transmitting channel synchronizes the transmit clock signal phase with the receive clock signal phase based on receive clock signal phase data.

20. The system of claim 19, further comprising means for transferring receive clock signal phase data from the receiving channel to the transmitting channel.

21. The system of claim 19, wherein the receiving channel and the transmitting channel are part of a transceiver.

22. The system of claim 21, wherein the transceiver includes a lane, the lane including both the receiving channel and the transmitting channel.

23. The system of claim 21, wherein the transceiver includes:
a first lane that includes the receiving channel; and
a second lane that includes the transmitting channel.

24. The system of claim 19, further comprising:
a first transceiver that includes the receiving channel; and
a second transceiver that includes the transmitting channel.

25. The system of claim 24, wherein the first transceiver and the second transceiver are disposed on a common substrate.

26. The system of claim 24, wherein:
the first transceiver is disposed on a first substrate; and
the second transceiver is disposed on a second substrate.
27. The system of claim 26, further comprising:
a board that includes both the first substrate and the second substrate.
28. The system of claim 26, further comprising:
a first board that includes the first substrate; and
a second board that includes the second substrate.
29. The system of claim 19, wherein the receive clock signal phase data includes a previous receive clock signal phase and a current receive clock signal phase.
30. The system of claim 19, wherein the receive clock signal phase data includes:
a phase difference between a previous receive clock signal phase and a current receive clock signal phase; and
a direction of the phase difference between the previous receive clock signal phase and the current receive clock signal phase.

31. A system for synchronizing a receive clock signal phase with a transmit clock signal phase, the system comprising:

a receiving channel that outputs a current receive clock signal pulse and receive clock phase data; and

a transmitting channel that includes a transmit clock signal and that receives the current receive clock signal pulse and the receive clock phase data from the receiving channel,

wherein the transmitting channel synchronizes the transmit clock signal phase with the receive clock signal phase based on the receive clock phase data.

32. The system of claim 31, further comprising means for transferring the current receive clock signal pulse and the receive clock phase data from the receiving channel to the transmitting channel.

33. The system of claim 31, wherein the receive clock phase data includes:

a phase difference between a previous receive clock signal phase and a current receive clock signal phase; and

a direction of the phase difference between the previous receive clock signal phase and the current receive clock signal phase.

34. The system of claim 31, wherein the receive clock phase data includes a previous receive clock signal phase and a current receive clock signal phase.

35. The system of claim 31, wherein the receiving channel includes a timing recovery module that receives a receive clock signal, stores a previous receive clock signal phase from the receive clock signal, and outputs the receive clock phase data based on a current receive clock signal phase and the previous receive clock signal phase.

36. The system of claim 31, wherein the transmitting channel includes a retiming module that receives the current receive clock signal pulse, the receive clock phase data, and a current transmit clock signal pulse, and outputs new transmit clock phase data based on the receive clock phase data.

37. The system of claim 36, wherein the retiming module includes a first-in-first-out register that receives the current receive clock signal pulse, the receive clock phase data, and a current transmit clock signal pulse, and outputs new transmit clock phase data based on the receive clock phase data,

wherein the receive clock phase data includes

a phase difference between a previous receive clock signal phase and a current receive clock signal phase; and

a direction of the phase difference between the previous receive clock signal phase and the current receive clock signal phase.

38. The system of claim 37, wherein the retiming module,
on the current receive clock signal pulse, receives and writes the receive clock phase data to the first-in-first-out register, and
on the current transmit clock signal pulse, reads out the new transmit clock phase data from the retiming module.

39. The system of claim 36, wherein the retiming module includes:
a first-in-first-out register that receives the current receive clock signal pulse, the receive clock phase data, and the current transmit clock signal pulse, and outputs the receive clock phase data; and
a phase calculator that receives the receive clock phase data from the first-in-first-out register and determines and outputs new transmit clock phase data based on the receive clock phase data.

40. The system of claim 39, wherein the receive clock phase data includes:
a phase difference between a previous receive clock signal phase and a
current receive clock signal phase; and
a direction of the phase difference between the previous receive clock
signal phase and the current receive clock signal phase.
41. The system of claim 39, wherein the receive clock phase data includes
a previous receive clock signal phase and a current receive clock signal phase.
42. The system of claim 41, wherein the phase calculator determines a
phase difference between the previous receive clock signal phase and the
current receive clock signal phase and also determines a direction of the phase
difference from the previous receive clock signal phase to the current receive
clock signal phase.
43. The system of claim 39, wherein the receive clock phase data includes:
a predetermined phase difference between a previous receive clock
signal phase and a current receive clock signal phase;
a direction of the phase difference between the previous receive clock
signal phase and the current receive clock signal phase; and
the previous receive clock signal phase and the current receive clock
signal phase.

44. The system of claim 43, wherein the phase calculator includes:

- a phase difference calculator, having an input and an output, that determines a phase difference and a direction between the previous receive clock signal phase and the current receive clock signal phase;
- a multiplexer, having an input coupled to the phase difference calculator output and having an output, that determines whether to output the phase difference determined by the phase difference calculator or the predetermined phase difference; and
- an add delta module, having an input coupled to the multiplexer output and having an output, that adjusts the transmit clock signal phase according to the multiplexer output.

45. The system of claim 43, wherein the phase calculator includes:

- a phase difference calculator, having an input and an output, that determines a phase difference and a direction between the previous receive clock signal phase and the current receive clock signal phase;
- a first multiplexer, having an input coupled to the phase difference calculator output and having an output, that determines, based on a phase control selection signal, whether to output the phase difference determined by the phase difference calculator or the predetermined phase difference;
- a second multiplexer, having an input coupled to the first multiplexer output, and having an output, that determines, based on a phase adjust decision signal, whether to output the first multiplexer output or zero; and
- an add delta module, having an input coupled to the second multiplexer output and having an output, that adjusts the transmit clock signal phase according to the second multiplexer output.

46. The system of claim 45, wherein the phase calculator further includes:
a decision module, having an input coupled to the first multiplexer output and having an output coupled to the second multiplexer input, that determines whether to adjust the transmit clock signal phase.
47. The system of claim 46, wherein the decision module receives as an input a predetermined phase threshold and determines whether the output of the first multiplexer has a value outside the predetermined phase threshold.
48. The system of claim 47, wherein the decision module receives as an input a phase limit signal that signifies whether to limit phase adjustment of the transmit clock signal phase regardless of the output of the first multiplexer.
49. The system of claim 46, wherein the decision module receives as an input a transmit phase lock signal that signifies whether to adjust the transmit clock signal phase.
50. The system of claim 49, wherein the transmit phase lock is set, signifying that the transmit clock signal phase is not to be adjusted, when switching data between a first transmit channel and a second transmit channel of a serializer/deserializer transceiver.

51. The system of claim 46, wherein the decision module includes a comparator having an input and an output, an AND gate having an input coupled to the comparator output and having an output, and an OR gate having an input coupled to the AND gate output and having an output coupled to the decision module output.

52. The system of claim 51, wherein:

the comparator receives at its input the first multiplexer output and a predetermined phase threshold;

the AND gate receives at its input a phase limit signal; and

the OR gate receives at its input a transmit phase lock signal and outputs a phase adjust decision signal.

53. The system of claim 45, wherein the second multiplexer outputs an adjustment value of zero if the phase adjust decision signal signifies that the transmit clock signal phase is not to be adjusted.

54. A method of phase-locking a transmit clock signal phase with a receive clock signal phase, the method comprising:

receiving a predetermined phase difference and direction between a previous receive clock signal phase and a current receive clock signal phase;

receiving the current receive clock signal phase;

store the current receive clock signal phase as a stored previous receive clock signal phase;

determining a calculated phase difference and direction between the previous receive clock signal phase and the current receive clock signal phase;

receiving a phase control selection signal;

selecting either the predetermined phase difference and direction or the calculated phase difference and direction as a selected phase difference and direction, depending on the phase control selection signal;

receiving a previous transmit clock signal phase; and

add or subtract, depending on the selected direction, the selected phase difference to/from the previous transmit clock signal phase to obtain an adjusted transmit clock signal phase.

55. The method of claim 54, further comprising:

receiving a predetermined phase threshold; and

determining whether the selected phase difference is outside the predetermined phase threshold.

56. The method of claim 55, further comprising:

receiving a phase limit signal that signifies whether to limit phase adjustment of the previous transmit clock signal phase regardless of whether the selected phase difference is outside a predetermined phase threshold.

57. The method of claim 56, wherein the adding step further includes the step of:

changing the selected phase difference to a value of zero if the selected phase difference is outside the predetermined phase threshold and the phase limit signal signifies that phase adjustment is to be limited.

58. The method of claim 54, further comprising:

receiving a transmit phase lock signal that signifies whether to adjust the previous transmit clock signal phase.

59. The method of claim 58, wherein the adding step further includes the step of:

changing the selected phase difference to a value of zero if the transmit phase lock signal is set.

60. The method of claim 54, further comprising:

receiving a predetermined phase threshold;

determining whether the selected phase difference is outside the predetermined phase threshold;

receiving a phase limit signal that signifies whether to limit phase adjustment of the previous transmit clock signal phase regardless of whether the selected phase difference is outside a predetermined phase threshold; and

receiving a transmit phase lock signal that signifies whether to adjust the previous transmit clock signal phase regardless of the phase limit signal.

61. The method of claim 60, wherein the adding step further includes the step of:

changing the selected phase difference to a value of zero if the transmit phase lock signal is set.

62. The method of claim 60, wherein the adding step further includes the step of:

changing the selected phase difference to a value of zero if the transmit phase lock signal is not set and the selected phase difference is outside the predetermined phase threshold and the phase limit signal signifies that phase adjustment is to be limited.